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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,207	01/20/2004	Darin Chan	50432-470	8068

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,207	CHAN ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed May 19, 2005.

Response to Amendment

The amendment to the specification is sufficient to overcome the objection to the specification stated in the previous office action. Therefore, this objection is withdrawn.

The limitations added to claims 1 and 10 are sufficient to overcome the rejections of claims 1, 3-11, 13 and 14 under 35 U.S.C. 102(e) as being anticipated by Yuzuriha (US 6,682,985), the rejections of claims 1-4, 6 and 9-12 under 35 U.S.C. 102(e) as being anticipated by Shimizu (US 6,846,721), the rejections of claims 2, 12 and 15 under 35 U.S.C. 103(a) as being unpatentable over Yuzuriha in of the admitted prior art, and the rejection of claim 15 under 35 U.S.C. 103(a) as being unpatentable over Shimizu in of the admitted prior art. Therefore, these rejections are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Tien (US 6,221,785, cited in IDS).

Regarding claim 1, Tien discloses forming a pad oxide layer (14) on a main surface of a substrate (12), forming a polish stop layer (16) on the pad oxide layer, forming an opening in the polish stop layer, pad oxide layer and an opening extending into the substrate, filling the opening in the substrate with a dielectric material (22) forming an overburden on the polish stop layer,

planarizing the overburden, etching to remove a portion of the dielectric material forming a step having a height substantially equal to the height of the remaining polish stop layer between the dielectric material and the remaining polish stop layer, and removing the polish stop layer (Fig. 2A-2F; col. 3, ln. 15 – col. 4, ln. 36).

Regarding claim 3, Tien discloses that the polish stop layer is silicon nitride (col. 3, ln. 20-22).

Regarding claim 4, Tien discloses that the dielectric layer is silicon oxide (col. 3, ln. 46).

Regarding claim 5, Tien discloses depositing the dielectric material by chemical vapor deposition on the polish stop layer filling the opening and forming the overburden (col. 3, ln. 40-61).

Regarding claim 6, Tien discloses planarizing the overburden by chemical mechanical polishing such that the upper surface of the dielectric material is coplanar with the upper surface of the polish stop layer (Fig. 2C, col. 40-45).

Regarding claim 10, Tien discloses forming a pad oxide layer (14) on a semiconductor substrate (12), forming a silicon nitride polish stop layer (16) on the pad oxide layer, etching to form an opening in the polish stop and pad oxide layers, etching to form an opening extending into the substrate, depositing a layer of silicon oxide (22) on the polish stop layer filling the opening in the substrate, conducting chemical-mechanical polishing such that an upper surface of the silicon oxide layer is substantially coplanar with an upper surface of the polish stop layer, etching to reduce the upper surface of the silicon oxide layer so that it is below the upper surface of the remaining polish stop layer by a distance substantially equal to the height of the remaining polish stop layer, and removing the polish stop layer (Fig. 2A-2F; col. 3, ln. 15 – col. 4, ln. 36).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tien (US 6,221,785) in view of the admitted prior art.

Regarding claims 2 and 12, Tien discloses forming the isolation regions between devices on an integrated circuit, but does not specifically disclose depositing a gate layer of polycrystalline silicon and etching the layer to form a gate electrode. However, Applicant's specification admits that the steps of depositing a polysilicon gate layer and patterning it to form gate electrodes is conventional (pg. 5, ln. 12-13). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form a polysilicon gate on the substrate of Tien because Tien discloses forming the isolation trenches of his invention such that they lie between devices on an integrated circuit and the admitted prior art states that these gate-forming steps are conventional.

Regarding claim 15, Tien discloses stripping the silicon nitride polish stop layer by using hot phosphoric acid, but does not disclose any additional details of the stripping process (col. 4, ln. 26-29). Applicant's specification admits that the stripping process used to remove the silicon nitride pad layer of their invention, is conventional (pg. 4, ln. 24-25). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the admitted prior art stripping process to remove the silicon nitride layer of Tien because Tien discloses using a hot phosphoric acid stripping process and because the admitted prior art states that this stripping process is conventional.

Claims 7, 8, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tien (US 6,221,785) in view of Doris et al. (US 6,905,941).

Regarding claims 7, 8, 13 and 14, Tien discloses etching a thickness of the dielectric material that is equal to the thickness of the polish stop layer, but Tien does not disclose the actual thickness of the removed dielectric material/polish stop layer (col. 4, ln. 17-21). Like Tien, Doris discloses a process of forming shallow trench isolation features on a substrate using a silicon nitride polish stop layer on the surface of the substrate. Doris teaches that this silicon nitride polish stop layer can successfully perform its polish stop function when its thickness is 50-120 nm (500-1200 Å) (col. 19-25). At the time of the invention, it would have been obvious to one of ordinary skill in the art to etch the dielectric material of Tien a thickness of 50-120 nm because Tien discloses etching a thickness of the dielectric material that is equal to the thickness of the polish stop layer and Doris teaches that this type of silicon nitride polish stop layer is preferable formed of a thickness of 50-120 nm.

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tien (US 6,221,785) in view of Uenishi et al. (US 20030003644).

Regarding claims 9 and 11, Tien does not disclose forming an oxide liner in the opening in the substrate before depositing the dielectric material (silicon oxide). Like Tien, Uenishi discloses a process of forming shallow trench isolation features on a substrate. Uenishi additionally discloses oxidizing the surface of the trench to form an oxide liner thereon. Uenishi teaches that it is advantageous to form this oxide liner because the liner recovers the damage done to the substrate during the trench etching while also lessening the stress that occurs between the substrate and the subsequently deposited silicon oxide trench fill material (paragraph 0087). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form an oxide liner in the trench of Tien because Uenishi discloses that the oxide liner provides

the benefits of eliminating the damage done to the inside of the trench by etching while also decreasing the stress between the substrate and the dielectric material fill.

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Komori (US 6,452,246) discloses forming a nitride polish stop layer on a substrate, etching trenches into the substrate, forming an oxide liner on the trench surface, filling the trench with dielectric material, using CMP to planarize the dielectric material, and etching the surface of the dielectric material of a thickness equal to that of the nitride polish stop layer.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
August 4, 2005

Michael Trinh
Primary Examiner
Act SPE